

With regard to the Bhattacharya reference, it is respectfully submitted that the reference discloses using a compressive titanium layer as its first titanium layer. Thus, like the Mizuhara et al. reference, the Bhattacharya reference does not disclose a wafer or a chip device as recited in amended claims 1 and 3. Instead, the reference discloses using a substantially titanium oxide layer as the first layer.

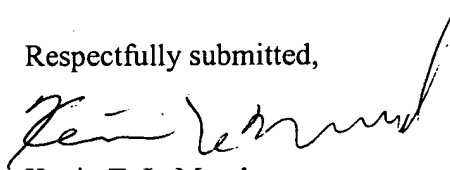
Accordingly, it is respectfully submitted that claims 1 and 3 are allowable for the above discussed reasons. Claim 2 depends on claim 1 therefore it is allowable for at least the reason claim 1 is allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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- 1 1. A wafer for use in a chip device comprising:
 - 2 a. a non-passivated wafer;
 - 3 b. a first substantially pure titanium layer;
 - 4 c. a first copper layer [above] directly on the first titanium layer;
 - 5 d. a second titanium layer [above] directly on on the first copper layer; and
 - 6 e. a second copper layer [above] directly on the second titanium layer.

- 1 3. A chip device comprising a wafer, the wafer comprising:
 - 2 a. a non-passivated wafer;
 - 3 b. a first substantially pure titanium layer;
 - 4 c. a first copper layer [above] directly on the first titanium layer;
 - 5 d. a second titanium layer [above] directly on the first copper layer; and
 - 6 e. a second copper layer [above] directly on the second titanium layer

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